## ABSTRACT OF THE DISCLOSURE

A freeway routing system for a field programmable gate array (FPGA). The system comprising a first FPGA tile. The first FPGA tile comprising a plurality of functional groups (FGs) arranged in rows and columns; a plurality of interface groups (IGs) surrounding the plurality of FGs such that one IG is positioned at each end of each row and column, each of the IGs having a first, second and third set of input ports and a first, second and third set of output ports; a freeway set of routing conductors configured to transfer signals to said first, second and third input ports, and configured to transfer signals from said first, second and third output ports of IGs in different PEG/IO/RAM; said freeway set of routing conductors comprising: a plurality of vertical conductors that form intersections with a plurality of horizontal conductors; and programmable interconnect elements located at said intersections in a diagonal orientation on said FPGA tile. It is emphasized that this abstract is provided to comply with the rules requiring an abstract that will allow a searcher or other reader to quickly ascertain the subject matter of the technical disclosure. It is submitted with the understand that it will not be used to interpret or limit the scope or meaning of the claims. 37 CFR 1.72(b).